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*hardware architecture is designed*

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*and developed on an FPGA-based  
(Field Programmable Gate  
Array-based) development platform.  
We perform experiments to evaluate  
our hardware architecture, in terms*



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*Information and Bioengineering,  
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*Information Technology has always  
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many aspects have to be considered*

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to learn, without being explicitly*

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*programmed and without human  
intervention. Machine learning  
algorithms can be categorized into  
supervised learning (classification)  
and unsupervised learning*

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(*clustering*). Among many

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*optimization algorithms that must solve compute-intensive problems under real-time constraints taking into account real-world parameters that evolve in time. Among others,*

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*evolutionary algorithms (EAs) are  
increasingly used in real-time  
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*Generation Michael Barrow<sup>1</sup>, Steven  
M. Burns<sup>2</sup> and Ryan Kastner<sup>1</sup>*

*<sup>1</sup>University of California, San Diego*

*<sup>2</sup>Intel Corporation, Hillsboro, OR*

*USA Abstract—Non-rigid 3D*

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classification and real-time object  
detection with high accuracy. The*

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*evaluation results show that our  
CNN-based FPGA accelerator can  
achieve 740 Giga operations per  
second (GOPS) at 200 MHz with  
kernel power of 12.2 watts on Intel*

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*16/1/2019 · In deep learning  
applications, FPGA accelerators  
offer unique advantages for certain*



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*use cases. In artificial intelligence applications, including machine learning and deep learning, speed is everything.. Whether you're talking about autonomous driving, real-time*

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*stock trading or online searches,  
faster results equate to better results.*

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*get the benefits of programmable  
logic without the cost, but with better  
latency, throughput, and power  
characteristics. With an eFPGA, you  
define the quantity of look-up-tables*

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*(LUTs), registers, embedded  
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*neural network accelerator based on  
an FPGA for the network model in  
Sect. 2. In this section, we introduce  
the overall architecture and the  
implementation of each module of*



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*Keywords: FPGA, Low Power,  
Object Detection, Real-Time 1*  
*Introduction Researchers in industry  
and academia have been striving for*

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*accurate and real-time pedestrian  
detection (PD) for more than a  
decade owing to many commercial  
and military applications. Industries  
such as surveillance, robotics, and*

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*various accelerators based on  
FPGA, GPU, and even ASIC design  
have been proposed recently to  
improve performance of CNN*

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*designs [3] [4] [9]. Among these approaches, FPGA based accelerators have attracted more and more attention of researchers because they have advantages of*

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*good performance, high energy efficiency, fast development round, and*



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...

*between the two interdependent  
criteria [10]. Focus on one aspect  
while ignoring the other, is bound to  
result in a sub-optimal architecture.*

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*In this paper, we present a systematic approach for the design and development of an FPGA-based DCNN accel-erator. Speci cally, we*

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*13/7/2020 · By processing the real-time tasks for the motion control in an FPGA, a standard PC without real-time OS can be used. The FPGA*

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*is the Accelerator For most  
applications, standard processors  
provide more than enough computing  
power. Nevertheless, there are still  
many applications where an external*

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*accelerator is needed.*

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*points of the accelerator templates,  
without detailing the hardware  
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*architectural template consists of two parts: the stream interface unit and the data path (Figure 2). The stream interface unit consists of one or more input and output stream modules,*

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architectures Carlos Valderrama is,  
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implement the spectrogram  
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*and distribute it via LimeNET Store,"  
says developer Gaspar Karm of his  
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LimeSDR family's field-*

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*The purpose of this would be to  
allow - so to speak - real-time  
execution of source code (or  
intermediate representation code), in*



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*the sense that you: Configure the  
FPGA to be a compiler for a specific  
language (C, for example) Feed the  
compiler with the source code for  
your program. The (machine code)*

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*output of the compiler goes directly  
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accelerators are often used to offload  
new and emerging workloads at an*

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*early stage of the deployment. Before  
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demonstrated by application to the  
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*WiFi. The remainder of this paper is structured as follows. Sections 2 and 3 outline the multi-SIMD accelerator design problem, before Sections 4*

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*reasons. First, they are very often characterized by a very regular, clock-level timing behavior: they behave similarly to state machines that evolve at each clock beat and*

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*hence, when running in isolation,  
their execution manifests very little*

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*timing fluctuations.*

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system consists of Nios II processor*

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*and stream-oriented dedicated  
hardware accelerators running at  
MHz clock rate, ... or patches of  
image pixels from one frame as  
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*Streaming 60 fps for real-time video  
streaming 7x greater than x265 slow  
... zone/accelerator-program.html  
Cloud End Users AWS F1 Apps and*

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*Libraries*

**Architectural Synthesis of Multi-**

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**SIMD Dataflow ...**

*3) Automatic AS of accelerators with  
demanding real-time requirements is  
demonstrated by application to the  
design of transceivers for 802.11n*

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*WiFi. The remainder of this paper is structured as follows. Sections 2 and 3 outline the multi-SIMD accelerator design problem, before Sections 4*

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*and 5 ...*

**FPGA Build an Open, Next-**



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## **Generation Virtualized Radio ...**

*macro cell capacity, FPGA-based accelerators are often used to offload new and emerging workloads at an early stage of the deployment. Before*

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*hardening its functions for further  
unit-cost reduction, Intel FPGA  
reference designs and IP help  
operators achieve a fast time-to-*

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*market trial or deployment.*

**Implementing a real-time, run-**

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## **time compiler on an FPGA ...**

*The purpose of this would be to  
allow - so to speak - real-time  
execution of source code (or  
intermediate representation code), in*

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*the sense that you: Configure the  
FPGA to be a compiler for a specific  
language (C, for example) Feed the  
compiler with the source code for  
your program. The (machine code)*

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*output of the compiler goes directly  
into ...*

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**Time-predictable hardware  
acceleration: we should not ...**

*5/8/2020 · Differently from other  
solutions, FPGA-based accelerators  
are particularly suitable for timing*

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*predictability for at least two main reasons. First, they are very often characterized by a very regular, clock-level timing behavior: they behave similarly to state machines*



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*that evolve at each clock beat and  
hence, when running in isolation,  
their execution manifests very little*

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*timing fluctuations.*

**Co-Designed FreeRTOS Deployed**

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**on FPGA**

*FreeRTOS, Hardware Accelerators.*  
*I. INTRODUCTION Real-time  
systems are typically present in  
embedded devices being designed to*

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*support time constrained tasks in meeting their deadlines. Depending on the need to meet strict deadlines, these systems can be classified in hard or soft real time [1]. In hard*

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*real-time applications, determinism  
and ...*

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